REMARKS

Claims 1-6 and 8-17 are currently active.

Claims 1 and 10 have been amended. Antecedent support for the amendment is found on page 1, line 11.

The Examiner has rejected Claims 1-6 and 10-16 as being unpatentable over Chan in view of Yamanaka. In view of the amendments to the claims, applicant respectfully traverses this rejection. The Examiner recognizes Chen does not teach the limitation "portions of packets as stripes" and cites Figure 1 of Yamanaka as teaching this limitation (see page 3, line 4 of the Office Action).

Referring to Yamanaka, there is disclosed a cell switching apparatus and a switching system. Yamanaka teaches outgoing-line speed adjustment buffers 23 are provided to each outgoing line. The outgoing line speed adjustment buffers are connected to the appropriate buffer memories according to an outgoing line space switch 14. The outgoing line space adjustment buffers 23 store the cell read out at a speed of more than R times of outgoing line speed from the buffer memory. The outgoing line speed adjustment buffers 23 transmits the stored cell to the associated outgoing line according to the outgoing line speed. The incoming line speed adjustment buffers 24 are provided to each incoming line. The incoming

line speed adjustment buffers 24 store the cell output from the associated header processing circuit. The incoming line speed adjustment buffers 24 read out the stored cell at W times of the incoming line speed and transfers the cell to an appropriate buffer connected by the incoming line switch 13. An access controller 100 has a writing buffer selector circuit 16, a read out buffer selective circuit 19 and a schedule controller 101. The access control 100 controls the writing buffer selective circuit 16 in the read out buffer selective circuit 19 by using these select scheduling controller 101. See column 10, line 64-column 11, line 20.

As shown in figure 1, the data is received on incoming lines of incoming buffers 24 where they are provided to the incoming line space switch 13 from the incoming line space switch. The data is provided to the buffer memory 11 which can provide it in turn to the outgoing line space switch 14. From the outgoing space switch 14, the data is provided to the outgoing line speed adjustment buffers 23 which then provide the data to the outgoing lines. In regard to amended Claim 1, there is not taught or suggested the limitation that "each fabric of the plurality of fabrics sending or receiving portions of a packet as stripes to or from the port card at a same logical clock cycle". Because Yamanaka teaches to first receive the data at the incoming line space switch 13 and only later in time does the outgoing switch 14 receive the same data, and not "at a same logical clock cycle," as found in Claim 1.

Furthermore, there must be some teaching or suggestion in the references themselves to combine the teachings the Examiner relies upon to arrive at applicant's claimed

invention. Besides the fact that amended Claim 1 has limitations which are not met by the applied art record, Chan has no need of switches at all, while Yamanaka requires switches. There is no reason why one skilled in the art would attempt to modify architecture of Chan with the teachings of Yamanaka this is so distinct. Furthermore, it would require significant research and development to even try to figure out how to modify the architecture of Chan to incorporate the incoming switch and outgoing switch architecture of Yamanaka to arrive applicant's claimed invention.

The only reason why one skilled in the art would combine these references is with hindsight. However, hindsight is not patent law. The Examiner cannot use the limitations of applicant's Claim 1 as a road map to find the different limitations in different references, and having found the different limitations in the different references, concludes that applicant's claimed invention is arrived at.

Moreover, the teachings of the references must be taken in the context in which they are found. The context of the teachings of Yamanaka are in regard to an incoming switch and an outgoing switch. The context of the teachings of Yamanaka are in regard to no switches whatsoever. Accordingly, these contexts cannot be ignored when combining these references, and can only result in the conclusion that these references cannot be combined. Accordingly, Claim 1 is patentable over the applied art of record.

Claims 2-6, 8 and 9 are dependent to Claim 1 and are patentable for the reasons Claim 1 is patentable.

Claim 10 is patentable for the reasons Claim 1 is patentable. Claims 11-18 are dependent to Claim 10 and are patentable for the reasons Claim 10 is patentable.

The Examiner has objected to Claims 9, 16 and 17.

In view of the foregoing amendments and remarks, it is respectfully requested that the outstanding rejections and objections to this application be reconsidered and withdrawn, and Claims 1-6 and 8-17, now in this application be allowed.

Respectfully submitted,

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